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AN INTERFACE UNIT TO LINK A REAL-TIME ANALYZER WITH AN INCREMEN--ETC(U)
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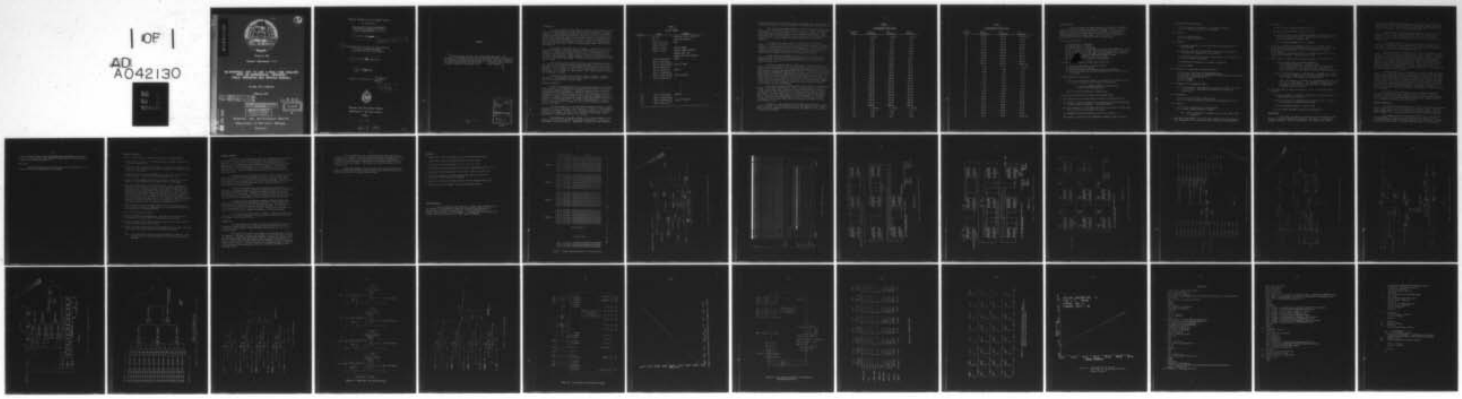

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Victoria, B.C.

Technical Memorandum 77-2

AN INTERFACE UNIT TO LINK A REAL-TIME ANALYZER WITH AN INCREMENTAL RECORDER (FIELD OPERATION AND SERVICE MANUAL)

R.C. Weir and K. Ashcroft

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Research and Development Branch

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ABSTRACT

A DREP-designed Interface Unit is described that links a PEC Incremental Tape Transport with a GR 1921 Real-Time Analyzer. The Interface Unit supplies the timing and control for the system. Four sets of signals are sampled periodically, and the resulting tape record is later used with a Sigma-7 computer to yield plots of dB versus frequency.

INTRODUCTION

The main components of the digital recording system described in this report are a General Radio 1921 Real-Time Analyzer, a Peripheral Equipment Corporation 1000/2000 Series Incremental Write Tape Transport, and a DREP-designed Interface Unit linking the two commercial units. The Interface Unit supplies the timing and control for the system, putting "housekeeping" and data pulses in proper sequence for recording on tape. Housekeeping information includes a start-of-record identifier, time pulses, channel numbers and gain-level code; data consist of frequency-band numbers and band levels (see Table 1).

The magnetic tape moves only on command. A recording is made every thirty-two minutes, its duration depending on the integration time of the analyzer. It consists of eight records for each of four channels, making thirty-two records in all. Signal levels and associated frequencies are recorded. Upon completion of this sequence, the tape stops moving and awaits the next thirty-two-minute command. Figure 1 gives an indication of the pattern of events.

On this basis, there can be forty-five recording periods each day, one 1200-foot tape running for about fifty-three days. For one tape this provides a total of almost 2,400 recordings, each of which has 8x4 records as described. It is possible, of course, to record oftener than every thirty-two minutes or to increase the time interval. Also, fewer than four channels can be sampled if desired.

Processing of the tape is done on a Sigma-7 computer. Because of the nature of the recording, several types of plot are easily obtained. These will be discussed later in the report.

GENERAL DESCRIPTION

In the following description of the data-gathering system, reference should be made to the simplified block diagram shown in Figure 2, as well as to the timing diagram in Figure 3. Signals at the four inputs to the data multiplexer are fed sequentially to the GR 1925 Multifilter, one of the components of the GR 1921 Real-Time Analyzer. The low-frequency multifilter consists of a bank of thirty, parallel, one-third-octave bandpass filters that have contiguous pass bands with centre frequencies ranging from 3.162 Hz (band 5) to 2.512 kHz (band 34). (See Table 2 and References 1, 2 and 3.) The pass bands with centre frequencies for the high-frequency multifilter are given in Table 3.

The filter outputs go to the GR 1926 Multichannel Detector, another component of the 1921 Analyzer. (See References 1, 4 and 5.) After sampling, the data are converted to binary form. The binary numbers go to a digital processor that computes rms level. Nine integration periods are possible, adjustable in octave steps from 1/8 to 32 seconds.

The band levels are stored in memory, to be made available, in BCD format, at the output of the GR 1921 Analyzer when required. Associated band numbers are also available. These data, accessed at a rate determined

TABLE 1

DIGITAL FORMAT

BYTE NO.	FORM	REMARKS
1	All 1's	Identifier (start reference)
2	All 1's	Identifier repeated
3	Binary (8 bits)	Time
4	Binary (8 bits)	
5	Binary (2 bits)	Channel number
6	Binary (2 bits)	Channel number repeated
7		Channel gain code
8		Channel gain code repeated
9	BCD (2 characters)	Band 5
10	BCD (2 characters)	
11	BCD (2 characters)	Level of Band 5
12	BCD (1 character)	
13	BCD (2 characters)	Band 6
14	BCD (2 characters)	
15	BCD (2 characters)	Level of band 6
16	BCD (1 character)	
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
125	BCD (2 characters)	Band 34
126	BCD (2 characters)	
127	BCD (2 characters	Level of band 34
128	BCD (1 character)	

by the timing-control circuitry, are fed to the output cards (11.71 to 11.78, inclusive) and thence to the PEC Incremental Tape Transport (see Reference 6).

The source of the timing control is a 1-MHz crystal oscillator that feeds a chain of dividers (cards 11.0, 11.1 and 11.2). Connections are made from card 11.2 to the output cards (11.71 to 11.78, inclusive); the same timing information goes to connector J3 for possible external use. Three time signals (25, 50 and 100 Hz) are taken from card 11.1 to provide cycling pulses (card 11.3) that sequence the various pulses through the output circuits.

A second set of inputs consists of gain-level voltages whose purpose is to indicate which step of gain in an automatic system is currently operative. Four dc voltages, one for each channel, are fed through low-pass filters to a multiplexer. The output of the multiplexer goes to an A/D converter whose binary outputs pass via the 11.7X output cards to the PEC tape transport to be recorded as part of the housekeeping information.

Channel selection is made by applying a high logic level to the appropriate logic input of the multiplexer; such is also the case with the signal channels. The logic highs are obtained from the channel-selector counter on card 11.6.

Operation commences when the START switch on the front panel of the Interface Unit is toggled on. Shortly afterwards, a 32-minute clock pulse causes the 1921 Analyzer to start sampling and integrating, visible indication being displayed on the front of the 1926 Detector. At the end of the integration period, an INTEGRATION COMPLETE signal is sent via card 11.5 to card 11.4, where timing control of the housekeeping and data pulses is initiated. Housekeeping and data enabling gates on card 11.3 are controlled from card 11.4. Cycling pulses T_1 to T_8, inclusive, are produced by card 11.3 from the 100-Hz, 50-Hz, and 25-Hz clock pulses. Also from card 11.3, the WRITE-STEP COMMAND is sent to the PEC Tape Transport, causing one row of parallel pulses to be recorded on tape for each command.

After each recording of band number and band level, an ADVANCE BAND signal is sent to the 1926 Analyzer. When all thirty bands have been recorded, a LAST BAND signal is returned from the 1926 Analyzer. The process is then repeated until thirty-two sets of data have been recorded, eight per channel. A counter keeps track of the number of completed integrations. After every eight, the logic operates to change the channel at the multiplexers. When the FINAL COUNT signal arrives, an inter-record gap (IRG) is generated and operation ceases until the arrival of the next 32-minute pulse from the clock.

Figures 4, 5 and 6 show the clock divider network; Figures 7,8,9 and 10 illustrate the circuits that do most of the timing control. Figure 11 gives the circuit diagram of the output cards; and Figure 12 is the circuit of the data multiplexer.

TABLE 2

LOW-FREQUENCY MULTIFILTER

Standard Band	Centre Frequency	Low Frequency	High Frequency
5	3.16 Hz	2.83 Hz	3.54 Hz
6	3.98	3.56	4.45
7	5.02	4.49	5.61
8	6.31	5.64	7.05
9	7.94	7.11	8.88
10	10.00	8.95	11.18
11	12.59	11.26	14.06
12	15.85	14.18	17.72
13	19.95	17.86	22.30
14	25.16	22.51	28.13
15	31.62	28.28	35.35
16	39.81	35.61	44.50
17	50.22	44.92	56.15
18	63.10	56.44	70.55
19	79.44	71.06	88.81
20	100.00	89.45	111.80
21	125.90	112.62	140.60
22	158.50	141.78	177.20
23	199.50	178.43	223.00
24	251.20	224.70	280.80
25	317.00	283.60	354.40
26	398.10	356.10	445.00
27	501.00	448.10	560.10
28	631.00	564.40	705.50
29	796.30	712.30	890.30
30	1000.00	894.50	1118.00
31	1.26 kHz	1.13 kHz	1.41 kHz
32	1.59	1.42	1.71
33	1.99	1.78	2.23
34	2.51	22.5	2.81

TABLE 3

HIGH-FREQUENCY MULTIFILTER

Standard Band	Centre Frequency	Low Frequency	High Frequency
20	100.00	89.45	111.80 Hz
21	125.90	112.62	140.60
22	158.50	141.78	177.20
23	199.50	178.43	223.00
24	251.20	224.70	280.80
25	317.00	283.60	354.40
26	398.10	356.10	445.00
27	501.00	448.10	560.10
28	631.00	564.40	705.50
29	796.30	712.30	890.30
30	1000.00	894.50	1118.00 Hz
31	1.26	1.13	1.41 kHz
32	1.59	1.42	1.71
33	1.99	1.78	2.23
34	2.51	2.25	2.81
35	3.16	2.83	3.54
36	3.98	3.56	4.45
37	5.01	4.48	5.60
38	6.31	5.64	7.05
39	7.94	7.106	8.88
40	10.00	8.95	11.18
41	12.59	11.29	14.06
42	15.85	14.18	17.72
43	19.95	17.85	22.30
44	25.12	22.47	28.08
45	31.62	28.28	35.35
46	39.81	35.61	44.50
47	50.10	44.81	56.01
48	63.10	56.44	70.55
49	79.44	71.06	88.81 kHz

TIMING SEQUENCE

A detailed sequence of timing events is given below. Reference should be made to the timing diagram given in Figure 3 and to the circuit diagrams, particularly Figures 7,8 and 9. Labelling of the integrated circuits is restricted to those whose identification is essential to an understanding of the following steps. F_1, F_2, F_3, and F_4 are SN7474N D-type flip-flops; all the rest are SN7476N J-K flip-flops.

1. Pre-start Conditions:

   (a) CLOCK output is inhibited.
   (b) DIVIDER chain is cleared.
   (c) CYCLING GATES are not cycling.
   (d) F1 is cleared: Q1 is NOT TRUE, inhibiting the HOUSEKEEPING gates.
   (e) F2 is preset; Q2 is TRUE, priming A1 and inhibiting the DATA gates.
   (f) F3 is cleared; Q3 is NOT TRUE, and the recorder is not stepping.
   (g) F4 is cleared; awaiting INTEGRATION COMPLETE signal.
   (h) INTE[illegible]ION COUNTER is preset to read ONE.
   (i) CH[illegible] SELECTOR is preset to select channel 1.

2. CLOCK o[illegible] is enabled by START switch opening A2:

   (a) WRITE-STEP FREQUENCY is present (200 Hz).
   (b) CYCLING GATES start cycling.
   (c) HOUSEKEEPING gates and DATA gates are still inhibited.
   (d) System is waiting for the START SAMPLING signal to arrive (every 32 minutes).

3. START SAMPLING signal arrives:

   (a) A pulse is produced at output Q of one-shot M1, resulting in the production of pulses at the outputs of one-shot M2:

      1. $\overline{Q}$ serves as CONVERT COMMAND for A/D converter.
      2. Q presets F5; Q5 becomes TRUE.

   (b) A3 is primed; awaiting the 2-second pulse.

4. Two-second pulse arrives, toggling F6; Q6 becomes TRUE.

5. The following 2-second pulse toggles F6 again; Q6 becomes NOT TRUE.

6. (a) A negative pulse is produced at Q of one-shot M3, starting operation of GR1921 Real-Time Analyzer. Measurement begins.

   (b) F5 is toggled, Q5 is NOT TRUE, and this circuit plays no further part until F5 is preset by another start pulse.

   (c) HOUSEKEEPING gates and DATA gates are still inhibited.

   (d) System is waiting for the INTEGRATION COMPLETE signal to arrive.

7. INTEGRATION COMPLETE arrives:

   (a) Pulse appears at M4 output; A4 is primed; awaiting T4.
   (b) F7 is cleared through M5; A5 is disabled.

8. T4 arrives:

   (a) F4 is toggled via A4.
   (b) A6 is primed; awaiting T1.

9. T1 arrives:

   (a) A6 opens, toggling F1 (Q1 becomes TRUE) and presetting F3(Q3 becomes TRUE).

   (b) A1 opens, priming the HOUSEKEEPING gates, which are enabled in turn when each appropriate T pulse arrives.

   (c) Because F3 is preset, A7 opens, pulses appear at the output of M6, and the recorder is stepped.

   (d) Housekeeping information is recorded sequentially.

   (e) A8 is primed.

10. T8 toggles F2, through A8; Q2 becomes NOT TRUE:

   (a) A1 closes, inhibiting the HOUSEKEEPING gates.
   (b) DATA gates are enabled in turn when each appropriate T pulse arrives.
   (c) Data are recorded sequentially.
   (d) A9 is primed.
   (e) A10 is primed.

11. T4 toggles F3; Q3 becomes NOT TRUE:

   (a) A7 is inhibited, thus stopping the recorder for steps 5,6,7 and 8 of the cycling. (Recorder will restart when T1 presets F3 through A6.)

12. T5 opens A9.

   (a) Pulse from M7 to GR1921 advances band.
   (b) T6, T7, and T8 continue cycling but the recorder does not step.

13. T1 arrives:

   (a) A6 opens, presetting F3; Q3 becomes TRUE.
   (b) A7 opens, and the recorder is stepped.

   NOTE: Data are recorded in sequence until the last (30th) band is completed.

14. LAST BAND (from GR1921), via A11 and A12, toggles F7 and thus primes A5. (The arrangement of A11 and A12 was used to overcome false triggering.)

15. T5 arrives:

    (a) F8 is preset, priming A13 which awaits T7.

    (b) The INTEGRATION COUNTER registers a count.

    (c) THE FINAL COUNT of the INTEGRATION COUNTER is absent except during the final integration period. Therefore, A14 is enabled and F5 preset through M9; Q5 becomes TRUE.

    (d) An A/D CONVERT COMMAND pulse is produced.

16. T7 arrives, toggling F8 and producing a pulse at the output of M8.
    F1 is cleared (Q1 becomes NOT TRUE) and F2 is preset (Q2 becomes TRUE), maintaining HOUSEKEEPING gates closed and inhibiting DATA gates.
    F3 is cleared.
    F4 is cleared (Q4 becomes NOT TRUE); A6 is disabled and T1 will not now toggle F1 nor preset F3. Recorder will not step.

17. After a delay, a START pulse is initiated. There are two possibilities:

    (i) The 2-second pulse has already primed A3.
    F6 is toggled immediately. Q6 becomes TRUE.
    On the following positive excursion of the 2-second waveform F6 is toggled again. Q6 becomes NOT TRUE, toggling F5; Q5 becomes NOT TRUE. A START pulse initiates the next integration.

    (ii) If the 2-second pulse is down when A14 is enabled, F5 is preset but F6 is not toggled until the 2-second waveform goes positive. The remainder of the sequence follows as before.

    NOTE: The sequence (6) through (17) is repeated eight times for each of the input channels. The INTEGRATION COUNTER keeps tab on the number of integrations. After 8n (n=1,2,3) integrations a different channel is selected.

18. The FINAL COUNT is chosen to be 8,16,24, or 32. If the FINAL COUNT is present:

    (a) A14 is disabled. No further sampling will take place until the START SAMPLING pulse arrives.

    (b) A15 is primed; it is enabled when T5 arrives via A5. An Inter-record Gap (IRG) is generated through M10.

    (c) The INTEGRATION COUNTER is preset to ONE.

    (d) The CHANNEL SELECTOR is preset to select channel 1.

GAIN CHANGES

If this digital equipment is connected to a data-gathering system that has a stepped automatic-gain mechanism, some means of recording the changes is required. One way of doing this is to provide a dc voltage

level for each gain level, feed these to an A/D converter, and record the binary output as part of the housekeeping information. Later, the binary numbers can be used to indicate the corrections that should apply during computer programming. This is the method used here.

Four gain-level signals are connected to the inputs of low-pass filters (Figure 13) whose outputs become the inputs to a multiplexer (Figure 14). The output of the multiplexer is fed to an A/D converter (Figure 15) and the resulting binary pulses go to the output cards (11.71 through 11.78).

The advantage gained in signal-to-noise ratio by using automatic gain must be weighed against the disadvantage of possible malfunction of this part of the system. Contamination of the coding signal by unwanted interference signals can lead to erroneous results.

Another thing to be considered is the effect of overshoot at the output of the gain-level 1-Hz low-pass filters. These filters are included to remove voltage fluctuations. Overshoot may not be a significant problem, especially since eight successive records are obtained for each channel, but its effect should be kept in mind. For example if short integration times are to be used it might be preferable to have 10-Hz low-pass filters instead of the 1-Hz filters presently in use. Also, adjacent gain levels should preferably be represented by voltages differing by one step only. Note that inverter-type amplifiers are used in the filters. This compensates for the inversion in the multiplexer.

A third possible source of trouble is the A/D converter and eight output cards. Should any one of the output cards develop a localized fault along the gain-code chain only, it might normally go undetected. As a check on this the program given in Appendix A, in addition to producing the main 32-record plot, yields a plot of gain-code binary number versus gain-level voltage (Figure 16). To utilize this feature, it is necessary to calibrate occasionally by feeding prescribed voltages to the gain-level inputs. The plot of Figure 16 was obtained by manually stepping the dc voltage 0.5 volts for every one of thirty-one records, starting with -7.5 volts and ending with +7.5 volts.

The reason for this discussion is not to suggest that problems will exist if an automatic-gain system is used, but rather to focus on possible trouble sources should anything go wrong. An additional safeguard is the inclusion of a second A/D converter whose output occupies the data "slot" immediately following that of the first.

STORAGE DISPLAY UNIT

The GR 1921-P1 Storage Display Unit is used to monitor the operation. Details concerning the unit can be found in References 7 and 8. A special cable connects socket AJ7 on the rear panel of the 1926 Detector with the REMOTE PROGRAM socket on the rear panel of the 1921-P1 Storage Display Unit.

This normally provides a fixed display rate that is not suitable for our purpose. Therefore, the wire supplying the X voltage to pin 1 of the REMOTE PROGRAM connector has been disconnected and taped back. The substituted time-base voltage is obtained from the output of a D/A converter

(Figure 17) whose inputs are the band-number pulses available at the inputs to the 11.7X output cards. The time-base voltage enters the display unit at a separate BNC connector marked 'X'.

Connections

A detailed wiring list is not given here, but the connection chart of Figure 18 may be of assistance in this regard.

OPERATING PROCEDURE

1. Put the START switch of the Interface Unit in the down position.

2. Apply power to all units: PEC tape transport, Interface, 1925 Multi-filter and 1926 Detector.

3. Thread the tape on the PEC tape transport, following the diagram on the front plate and ensuring that the tape is properly tensioned and fitted correctly in the guides.

4. Momentarily depress the LOAD FORWARD switch, observing the tape for a slight movement. If there is no movement repeat this step.

5. Depress the LOAD FORWARD switch again, holding it down until the tape comes to a controlled stop and the READY light is illuminated.

6. Raise the START switch of the Interface Unit. After a minute or so integration will commence. Housekeeping information, band numbers and band levels will be recorded on tape. This will be evident from the indications on the front panel of the 1926 Detector, a whirring noise from the PEC tape transport and slight motions of the tape. Thirty-two such sequences will occur. Visible operation then ceases until the start of the next set of integrations. The time interval between starts is thirty-two minutes,though this is easily altered. During this interval there will be several minutes of activity, depending in length on the selected integration time, followed by a quiescent period.

7. When sufficient records have been obtained or the tape supply reel is almost empty, flip down the START switch of the Interface Unit and wait for the arrival of a quiescent period.

8. Press the FILE GAP button twice.

9. Press the REWIND button momentarily. The tape will now rewind until the begining-of-tape tab (BOT) is reached and will then stop.

10. Press the REWIND control again and hold it down until the tape has been completely wound onto the supply reel.

11. Remove the supply reel and put the tape retainer over the reel. The tape is now ready for computer use with an appropriate program.

NOTE: It is important to keep the tape in a dust-free condition. Open the dust cover of the tape transport only when the tape requires changing.

COMPUTER PROGRAMS

Once the data are recorded on tape, the information can be displayed in a number of ways. What might be termed the basic program is given in Appendix A. This results in a plot similar to that shown in Figure 19, which is the full, uncorrected, 8x4 presentation of all the band levels and band numbers for eight integrations of all four channels. For the given example, the plots are of the outputs of a white-noise generator set at different levels. Figure 20 shows with more clarity one of the thirty-two individual plots.

The complete record shown in Figure 19 is called a physical record, and a file comprises an indefinite number of these. Thus, Figure 20 shows logical record No. 11 of the only physical record on the tape. Had there been twenty physical records on tape, and had it been desired to plot the ninth of the sequence, then LSKIP=8 would have been a required statement at the appropriate point in the program.

The word "uncorrected" was used in connection with the plot of Figure 19. It may be desired to introduce calibration factors into the program. For example, the overall gains of the circuit paths following the four data sensors may all be different. A CALFAC (calibration factor) can be built into the program for each channel. Again, if automatic gain is being utilized, a correction factor corresponding to the alteration of gain must be added.

In another form of presentation, for each channel the eight levels per band are averaged and plotted against band number. Hence, instead of thirty-two plots per physical record, there are only four. The plots from all of the physical records in a file can follow in sequence, or only those from a chosen range LSKIP to LMAX may be taken. The program to achieve this is not given here, but it is simply an extension of the basic program.

Other types of plots are easily obtained. These include plotting the level at a selected frequency over many physical records and plotting the gain changes over a period of time..

CONCLUSION

This memorandum has described a digital data-gathering system that periodically samples the signals of four channels and records levels with corresponding band numbers. Though designed several years ago, it is still a useful system.

The description given in this report is for operation in the field, as originally conceived. However, the equipment has also been used to analyze the outputs of a multitrack analog tape recorder. Because the playback speed was many times greater than the record speed, frequency multiplication took place. A higher-frequency multifilter was thus required, one that covered the bands shown in Table 3. For this operation, minor modifications are required in the program given in Appendix A, since the starting band number is now 20 rather than 5.

In this connection, too, a modification has been designed and installed by K. Ashcroft to remove the quiescent period (Figure 1) from the recording time sequence so that each physical recording is immediately followed in time by the next. Particulars of this modification have been omitted from this memorandum. The system can quickly be returned to its original state.

Among the advantages of such a system over analog recording are a higher signal-to-noise ratio, a large saving of tape, partially processed data, and a reduction in required operator time.

REFERENCES

1. General Radio Instruction Manual for Type 1921 Real-Time Analyzer.

2. General Radio Instruction Manual for Type 1925 Multifilter.

3. The General Radio Experimenter, Vol. 42 No.10, Oct. 1968.

4. General Radio Instruction Manual for Type 1926 Multichannel RMS Detector.

5. The General Radio Experimenter, Vol.43, Nos. 5 and 6, May/June 1969.

6. Peripheral Equipment Corporation Instruction Manual for 1000/2000 Series Incremental Write Tape Transport.

7. General Radio Instruction Manual for Type 1921-P1 Storage Display Unit.

8. Tektronix Instruction Manual for Type 601 Storage Monitor.

ACKNOWLEDGEMENTS

Valuable suggestions were made by J. Ganton, DREP, for whom the unit was designed and constructed. Though the Interface Unit was built by K. Ashcroft and the system assembled by him, R. Hale contributed to the testing and maintenance of the equipment. J. Dorscher supplied the subroutine READLG, which puts the data into a form usable by FORTRAN.

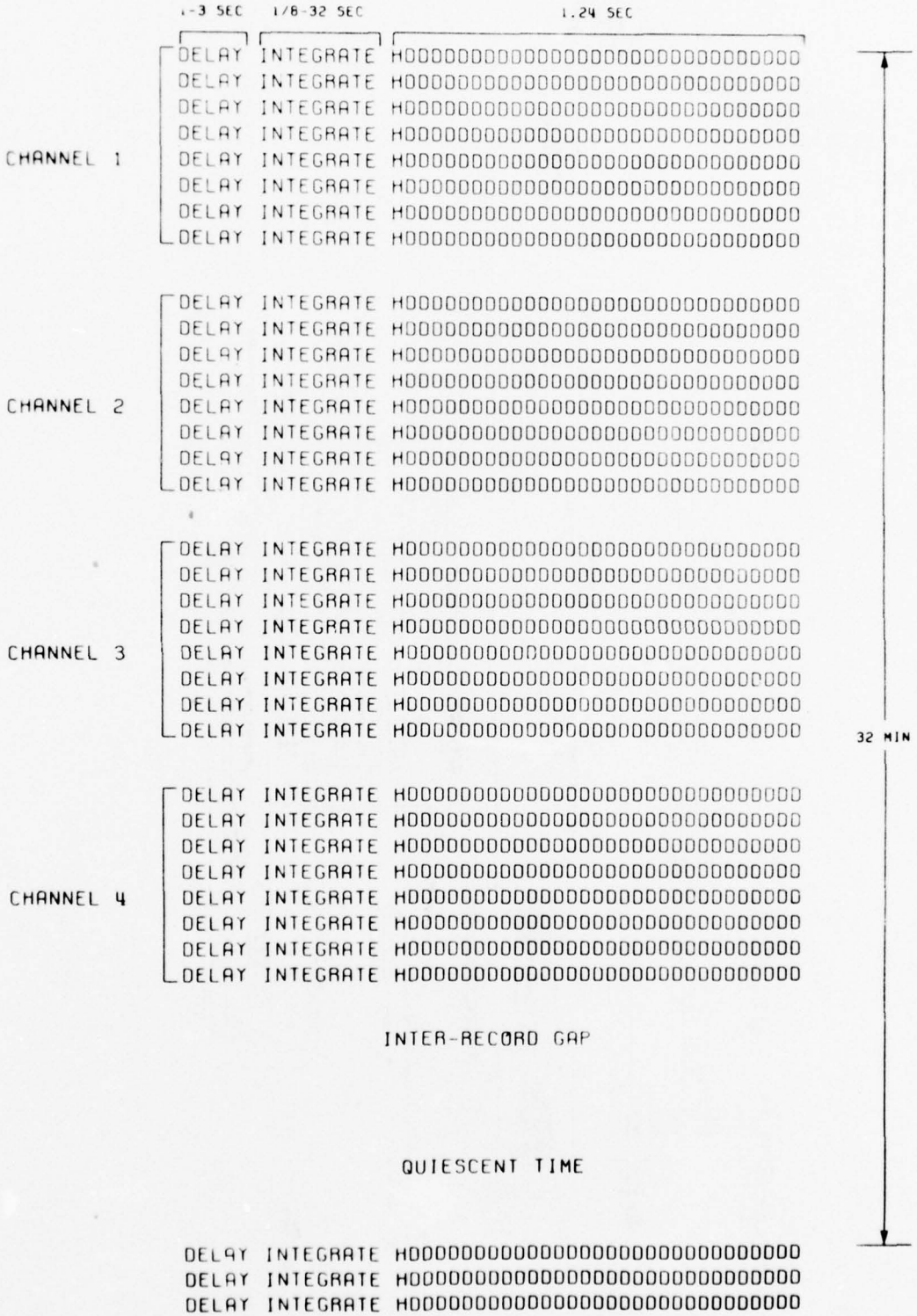


Figure 1. Pattern showing sequence of recorded pulses.

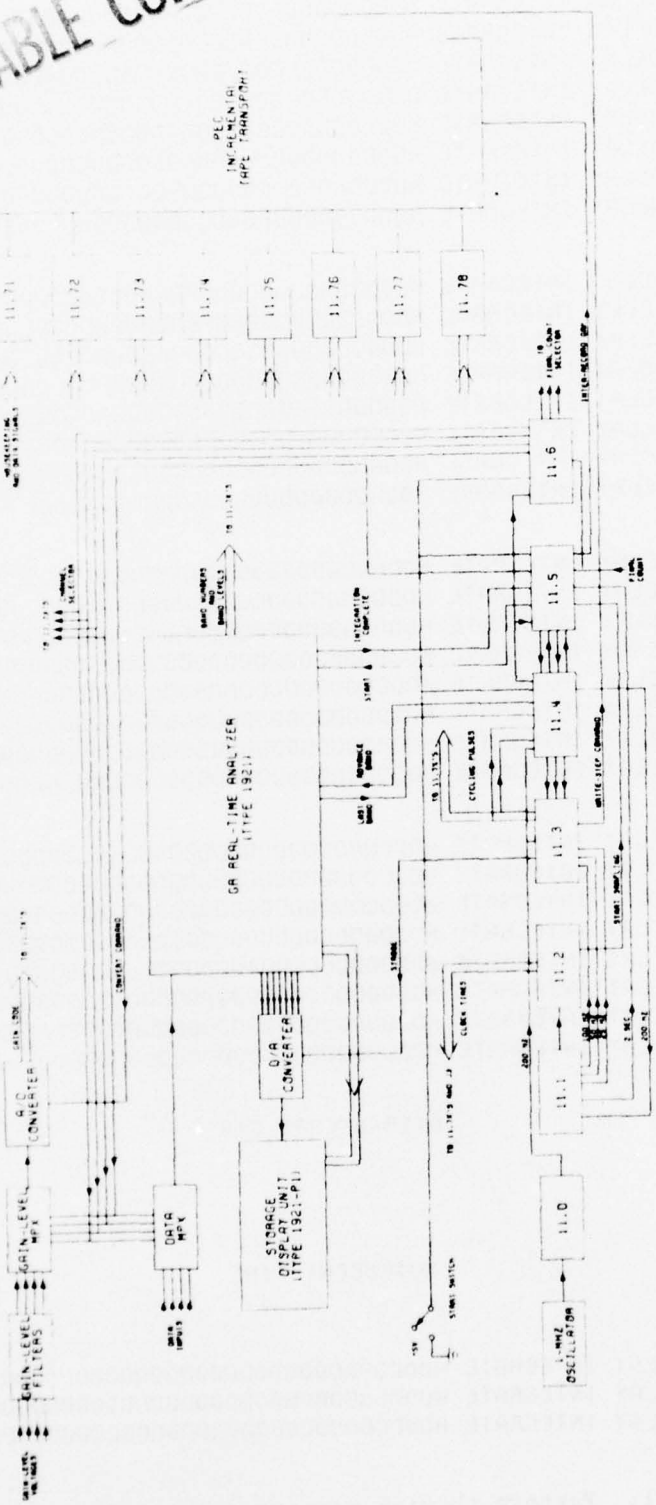


Figure 2. Block diagram of the data-gathering system.

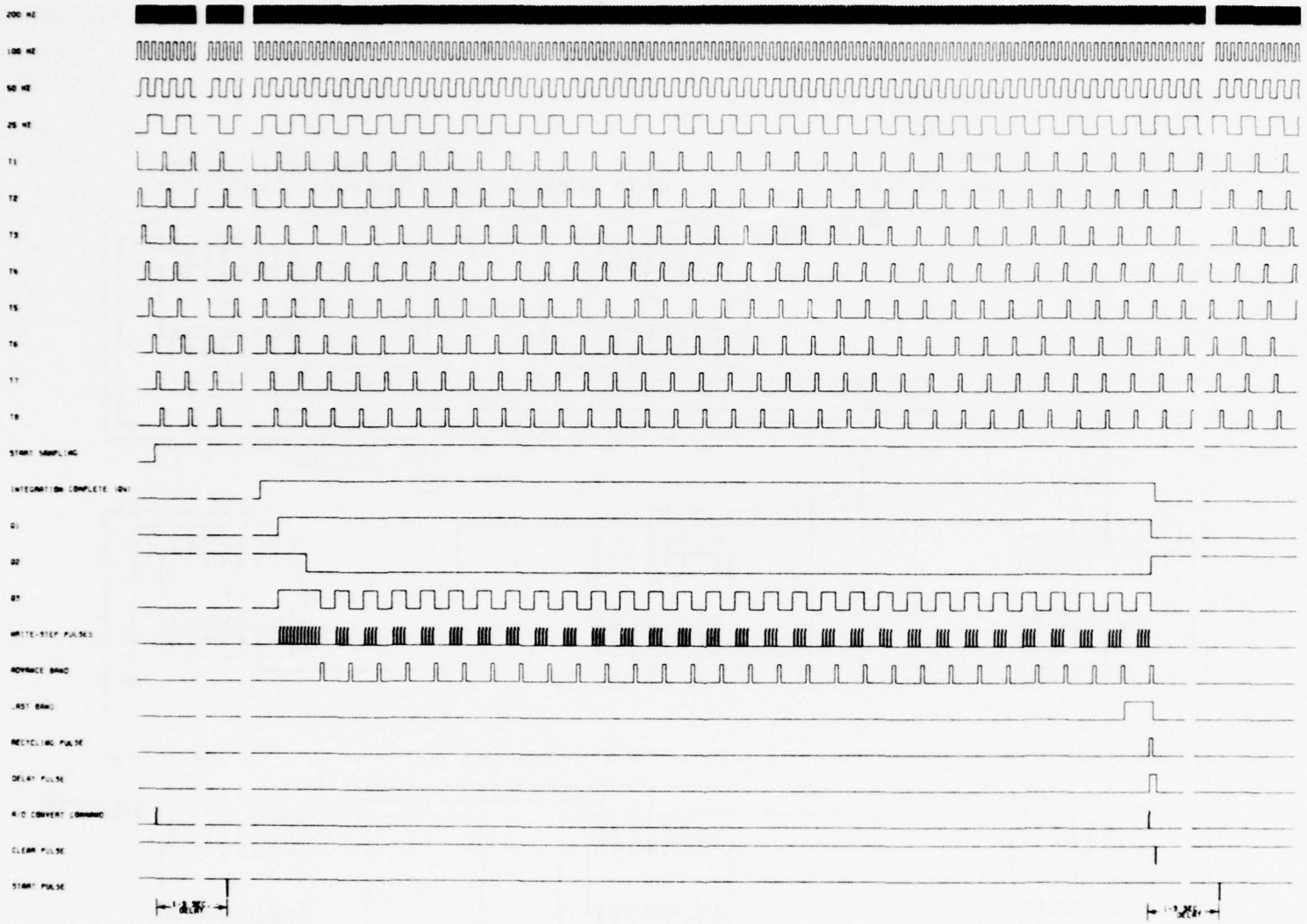


Figure 3. Timing diagram of events.

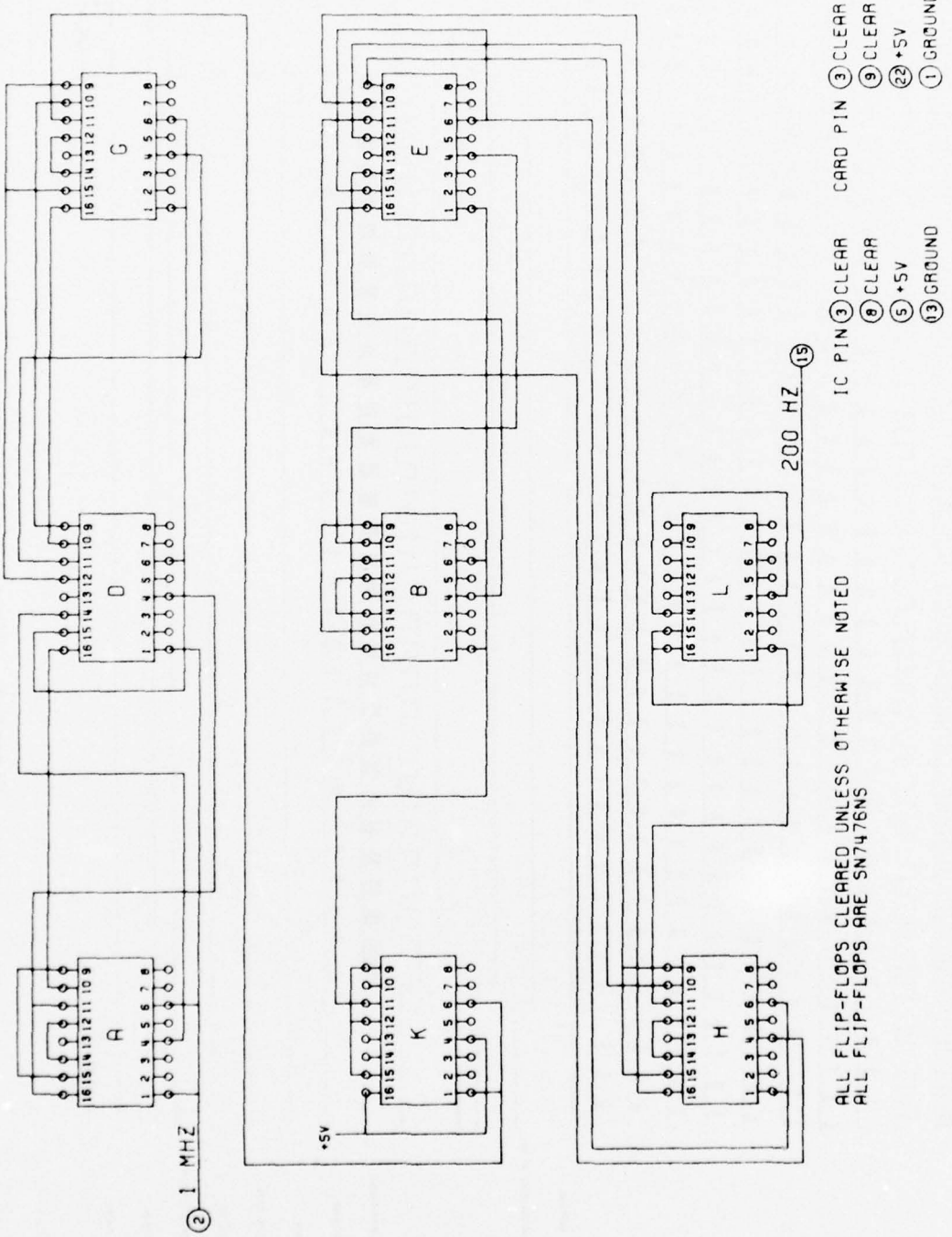


Figure 4. Diagram of circuitry mounted on card 11.0.

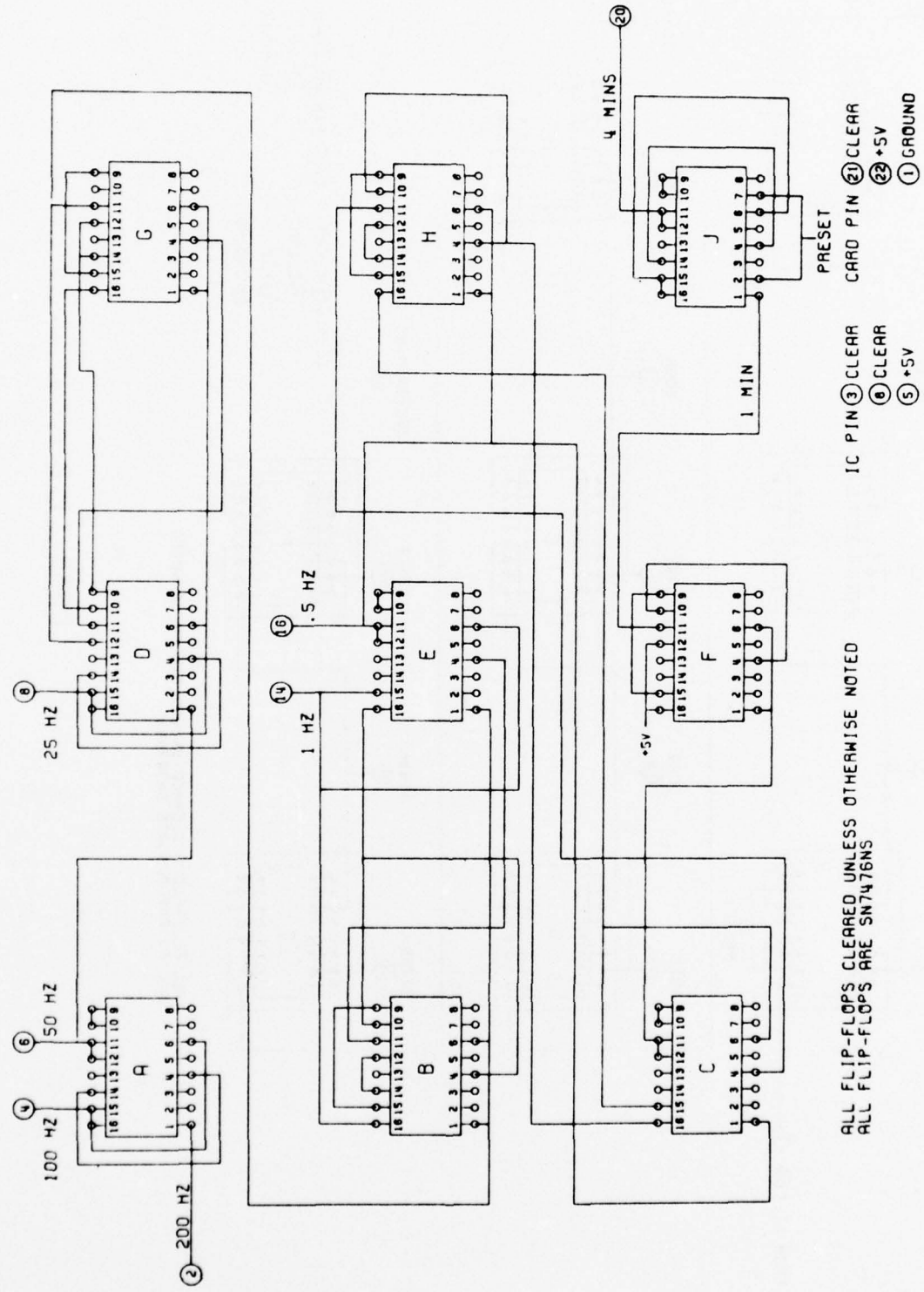
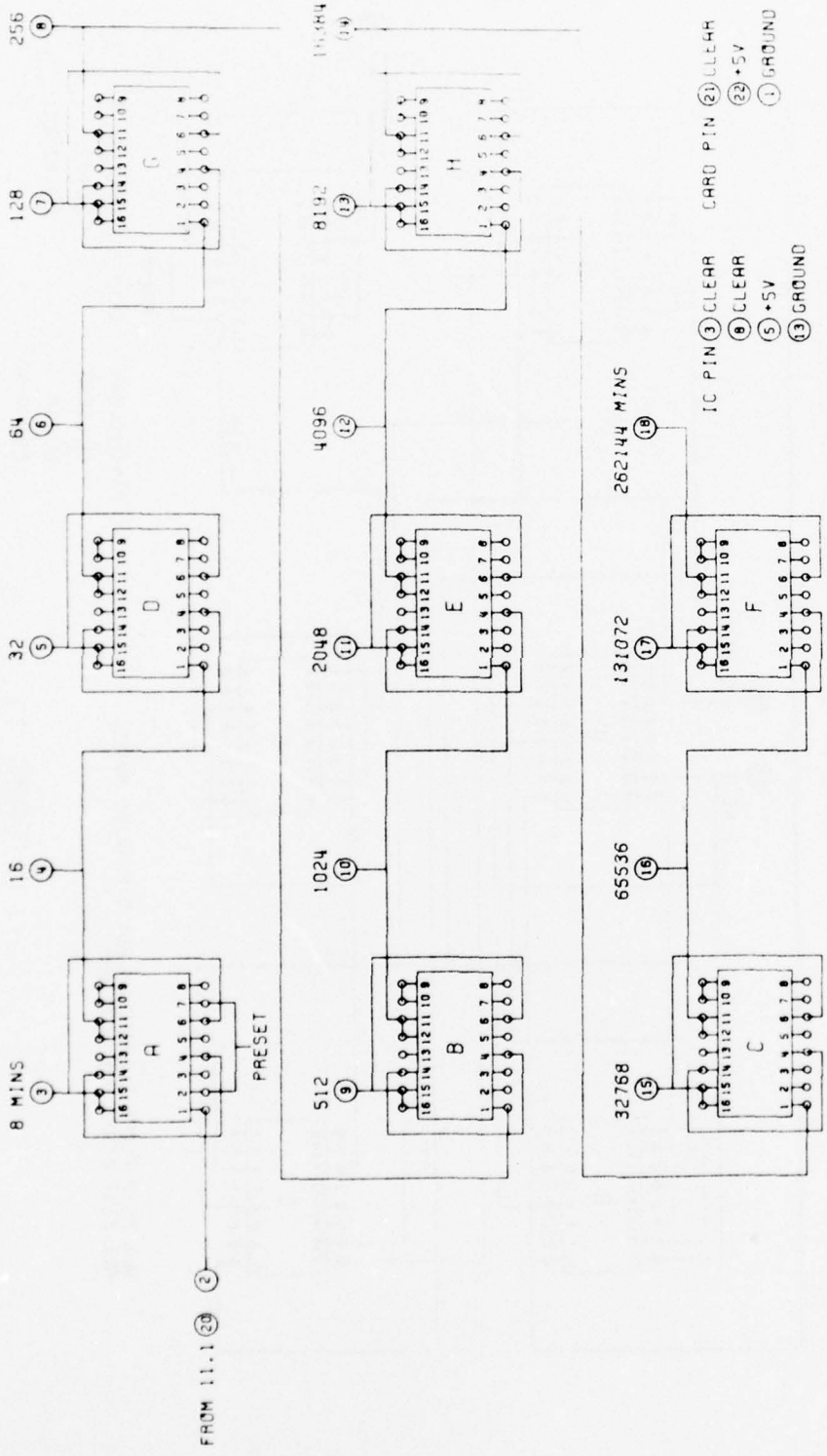


Figure 5. Diagram of circuitry mounted on card 11.1.



CARD 11.2

Figure 6. Diagram of circuitry mounted on card 11.2.

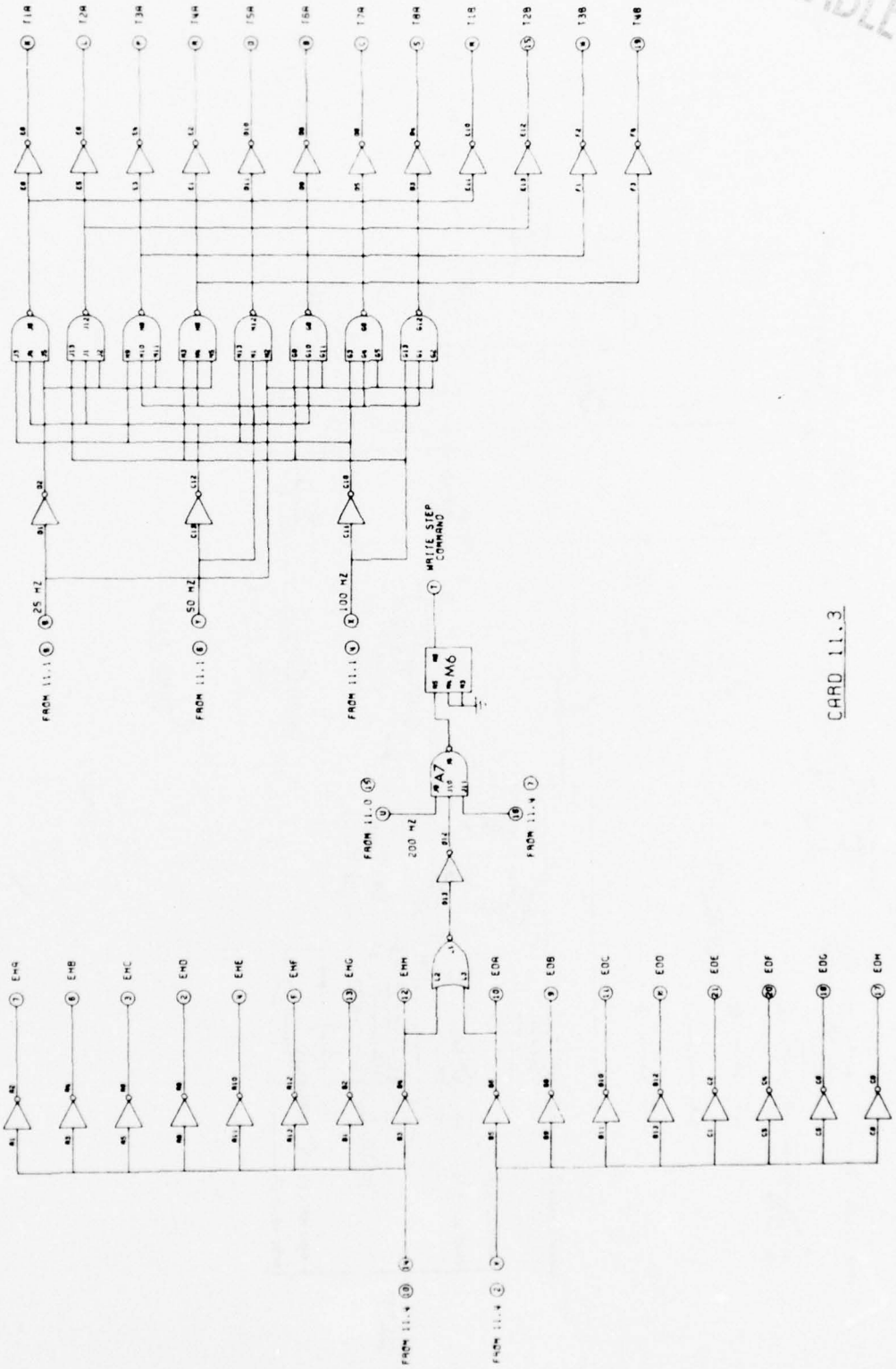
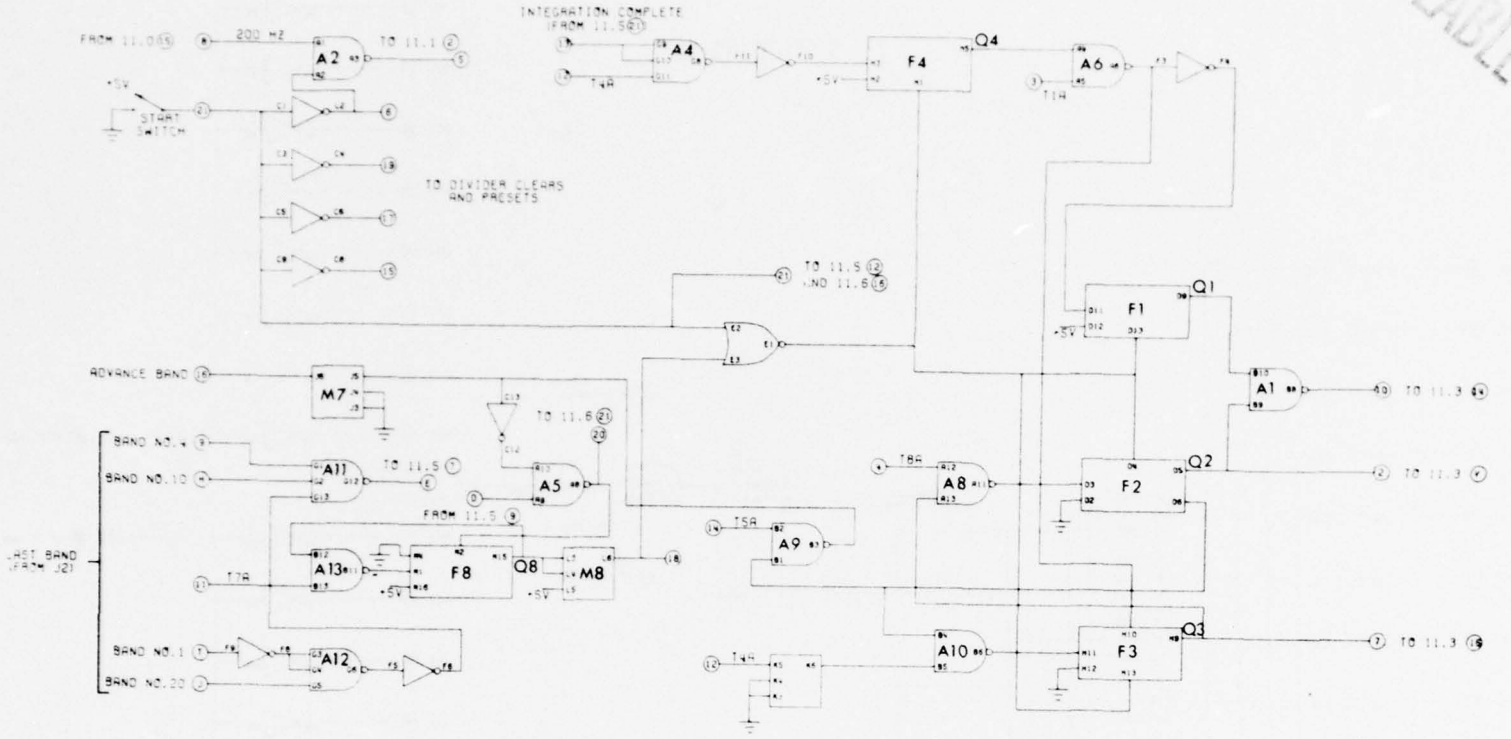
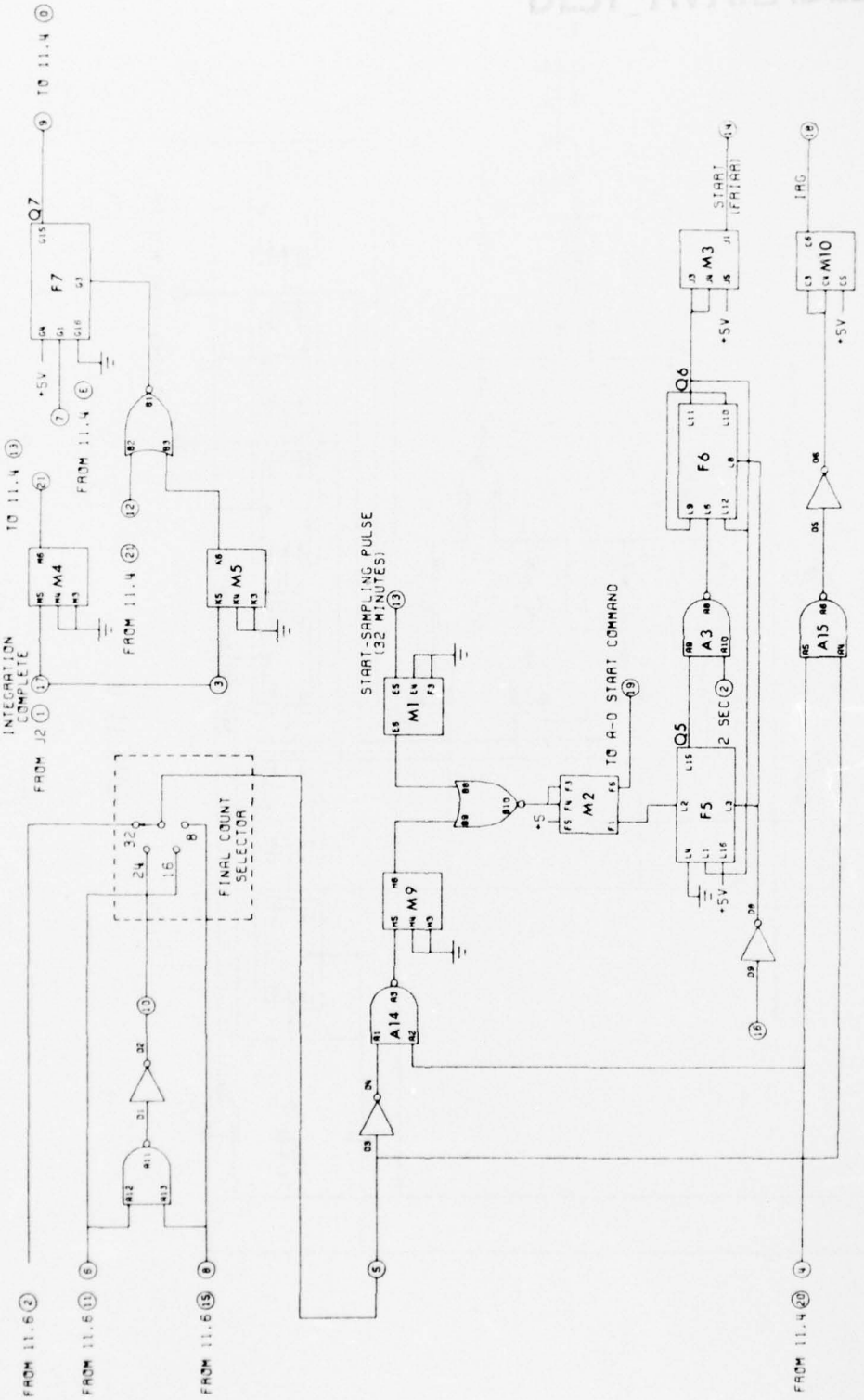


Figure 7. Diagram of circuitry mounted on card 11.3.



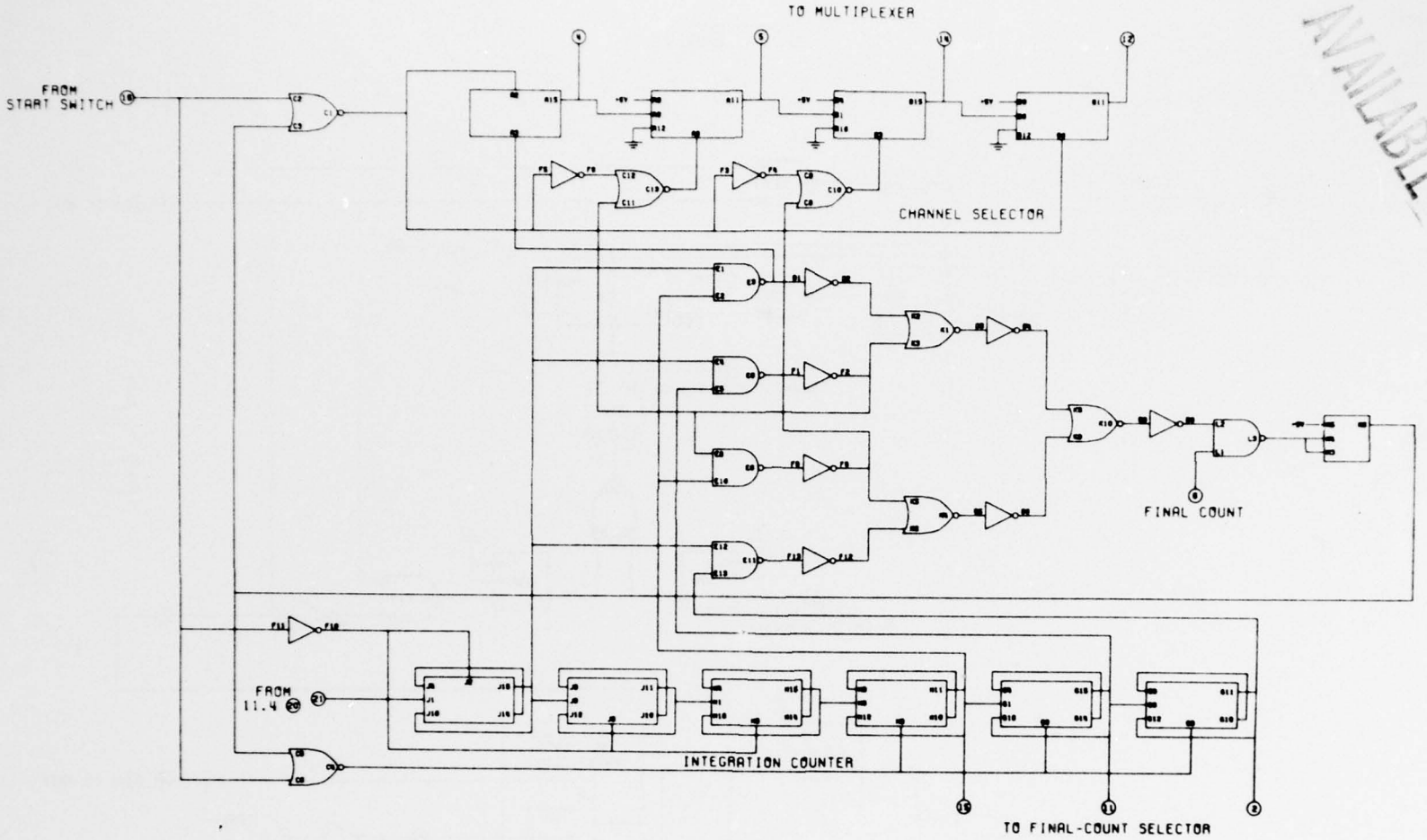
CARD 11.4

Figure 8. Diagram of circuitry mounted on card 11.4.



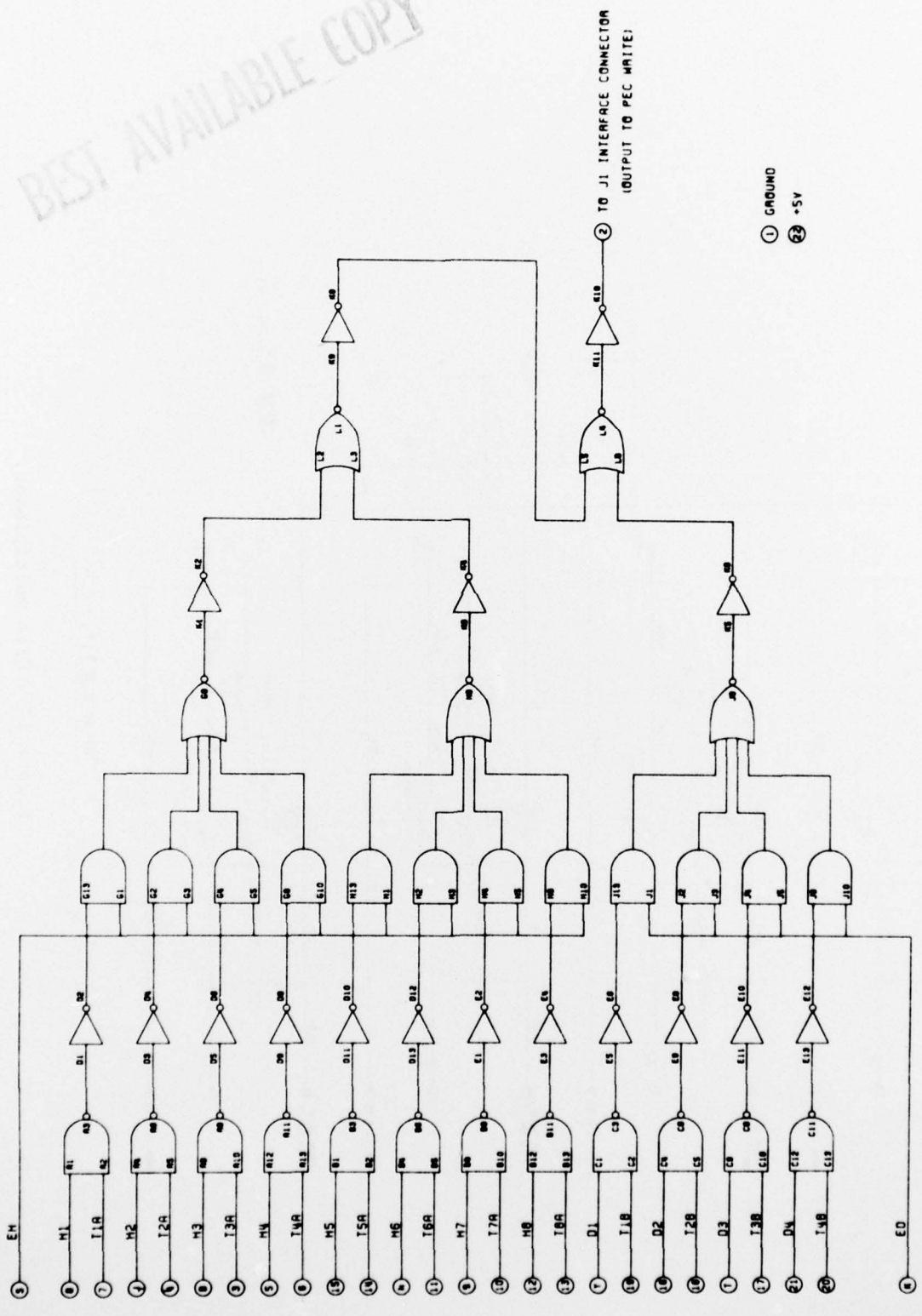
CARD 11.5

Figure 9. Diagram of circuitry mounted on card 11.5.



CARD 11.6

Figure 10. Diagram of circuitry mounted on card 11.6.



CARDS 11.71 THROUGH 11.78

Figure 11. Diagram of circuitry mounted on cards 11.71 to 11.78, inclusive.

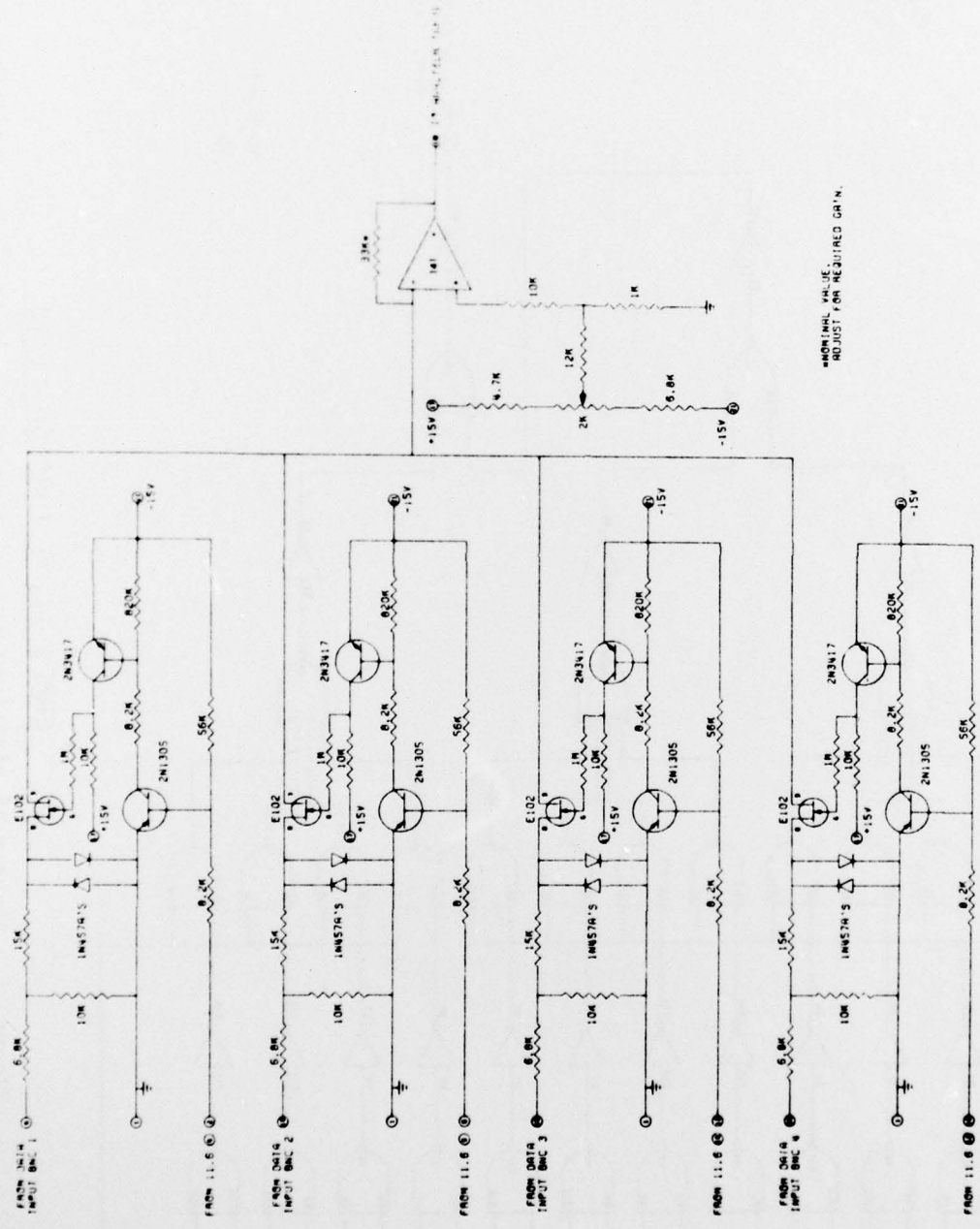
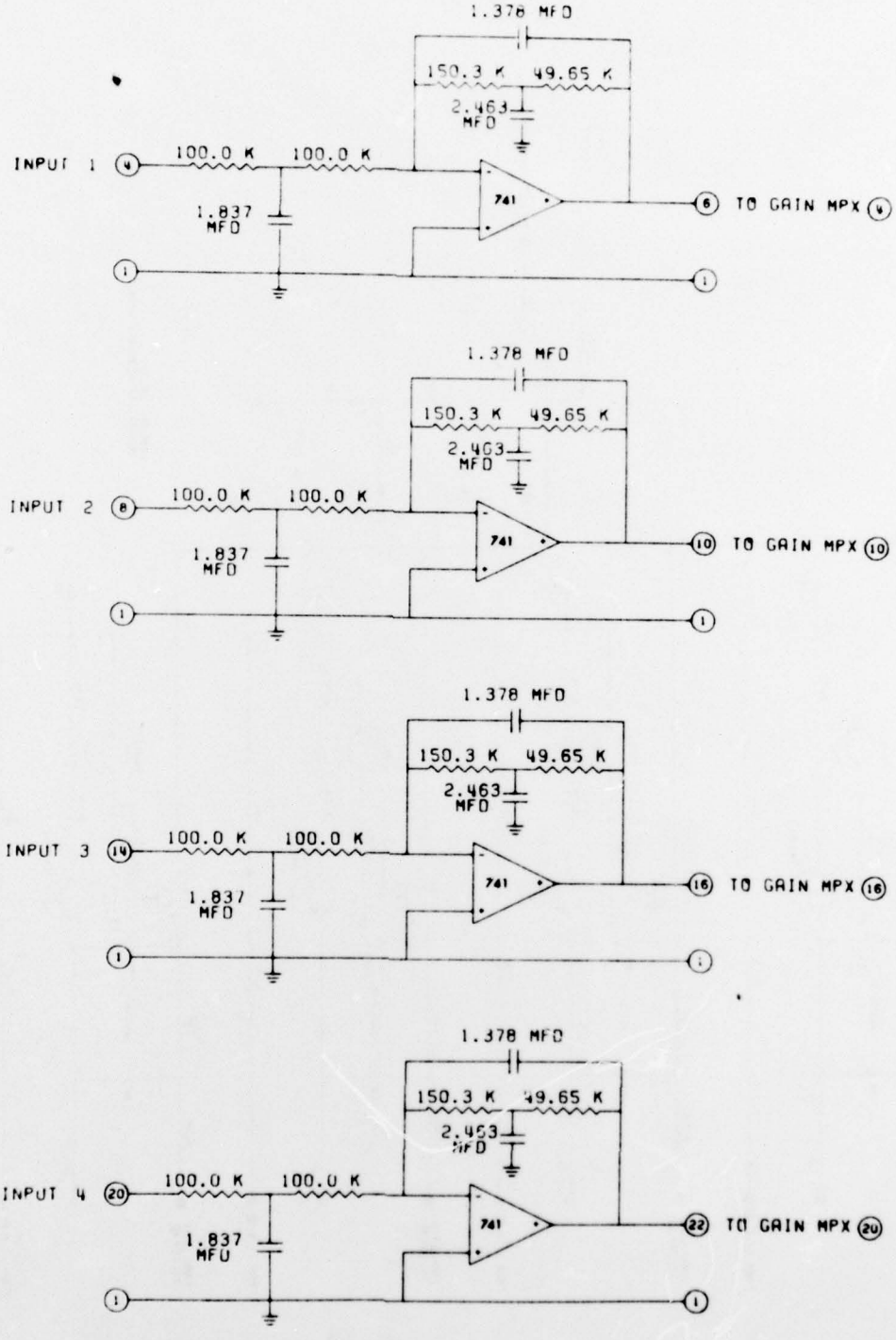


Figure 12. Data multiplexer.



GAIN-LEVEL FILTERS

Figure 13. Gain-level 1-Hz low-pass filters.

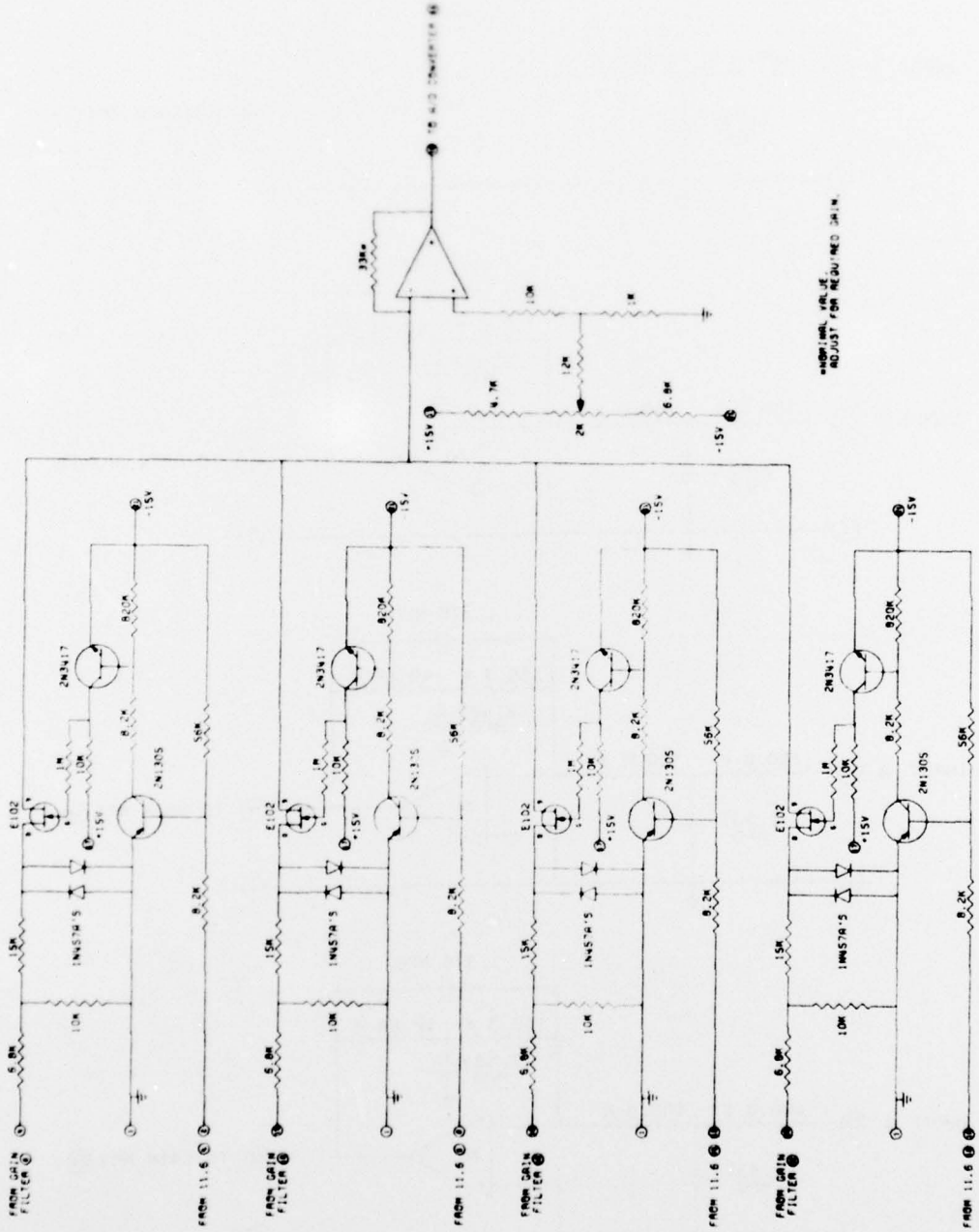


Figure 14. Gain-level multiplexer.

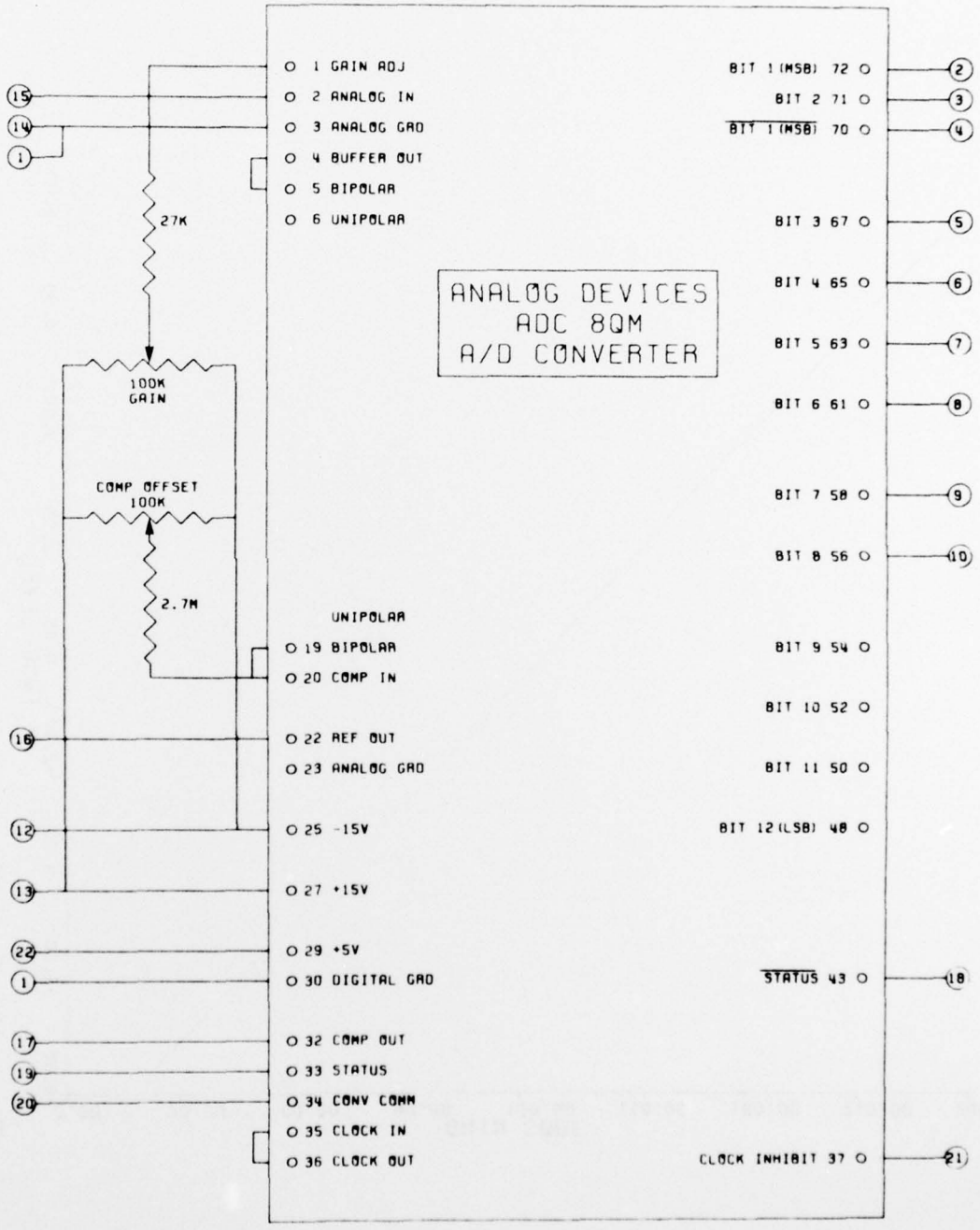


Figure 15. A/D converter for gain-level coding.

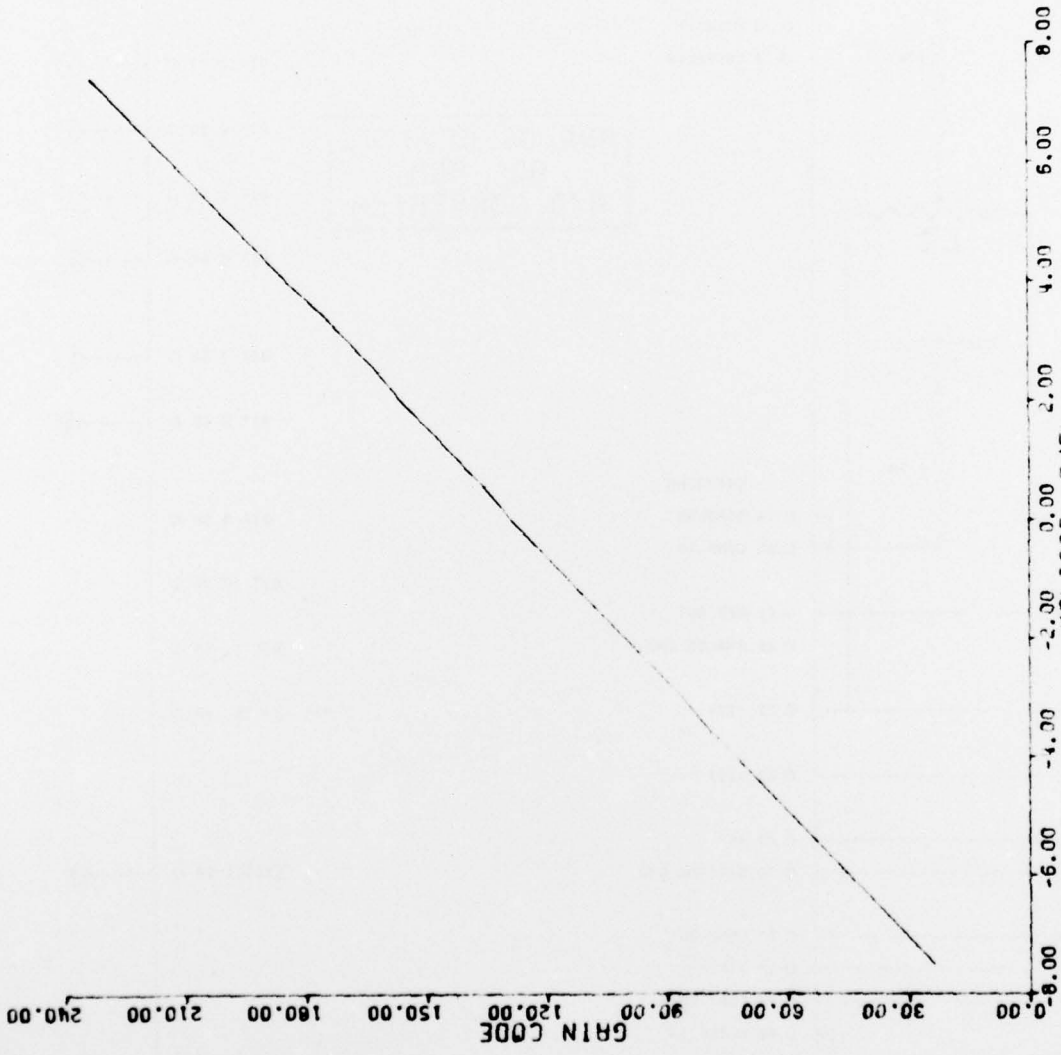


Figure 16. Gain-code output from A/D converter for stepped input voltage.

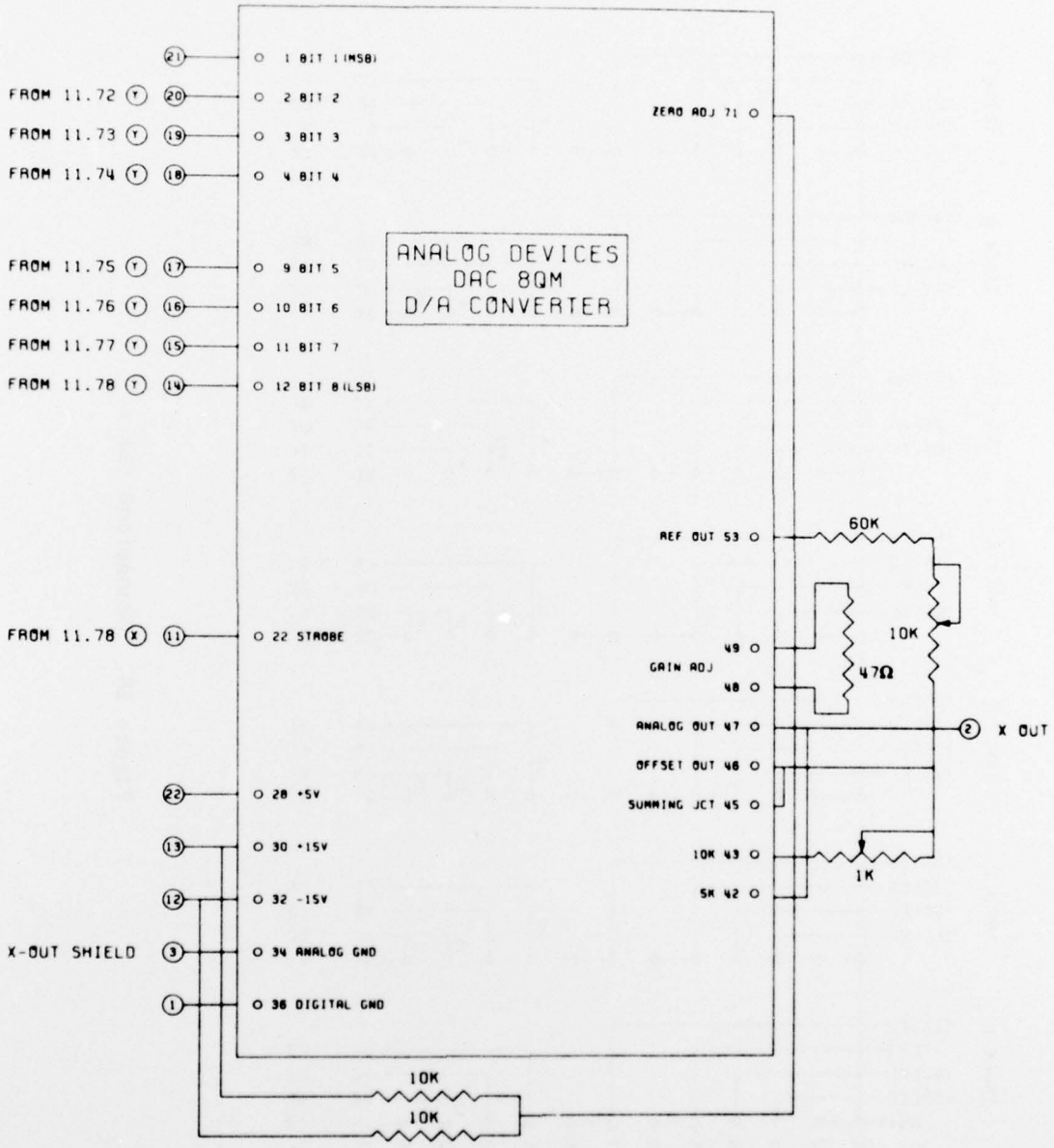


Figure 17. D/A converter supplying 'X' voltage to Storage Display Unit.

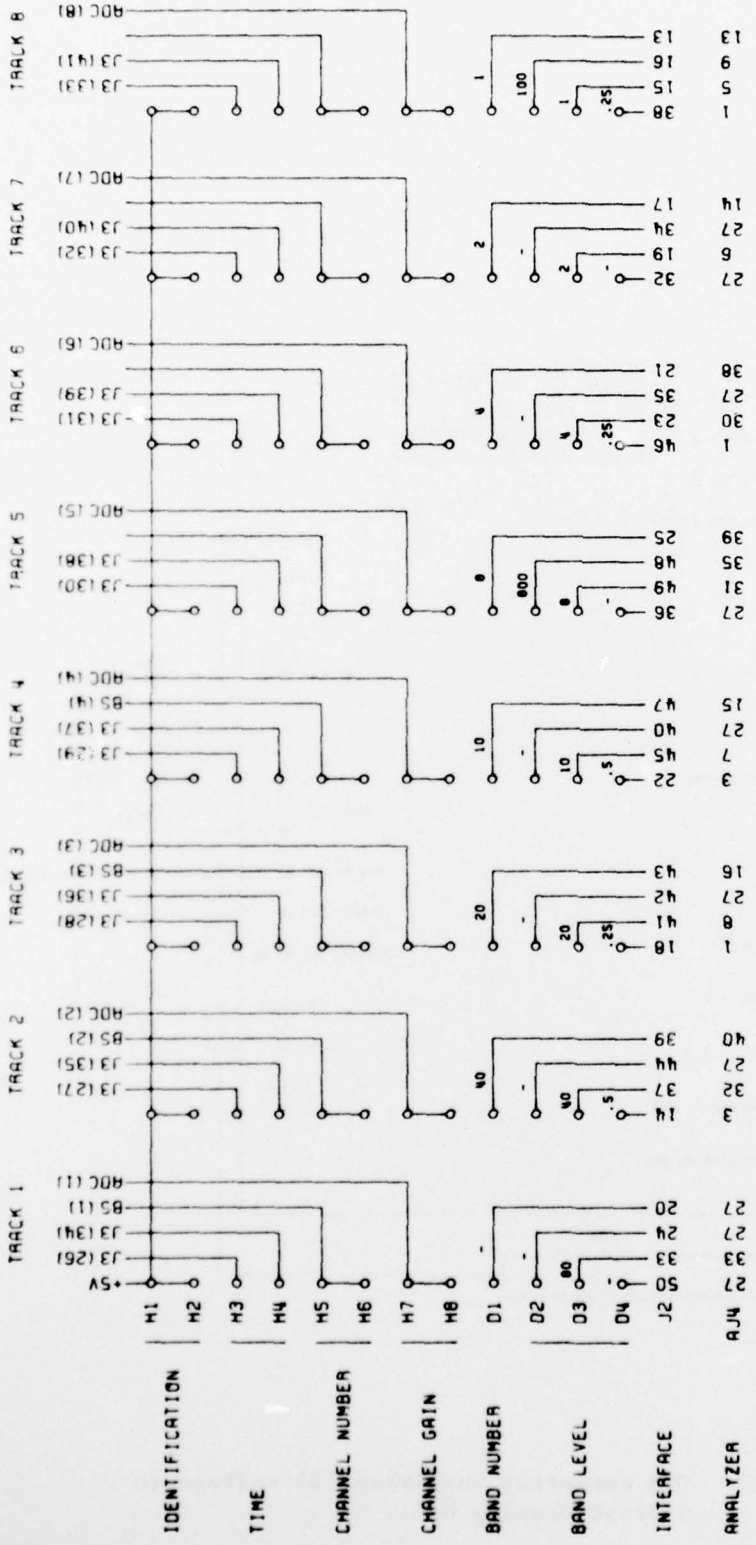


Figure 18. Connection Chart.

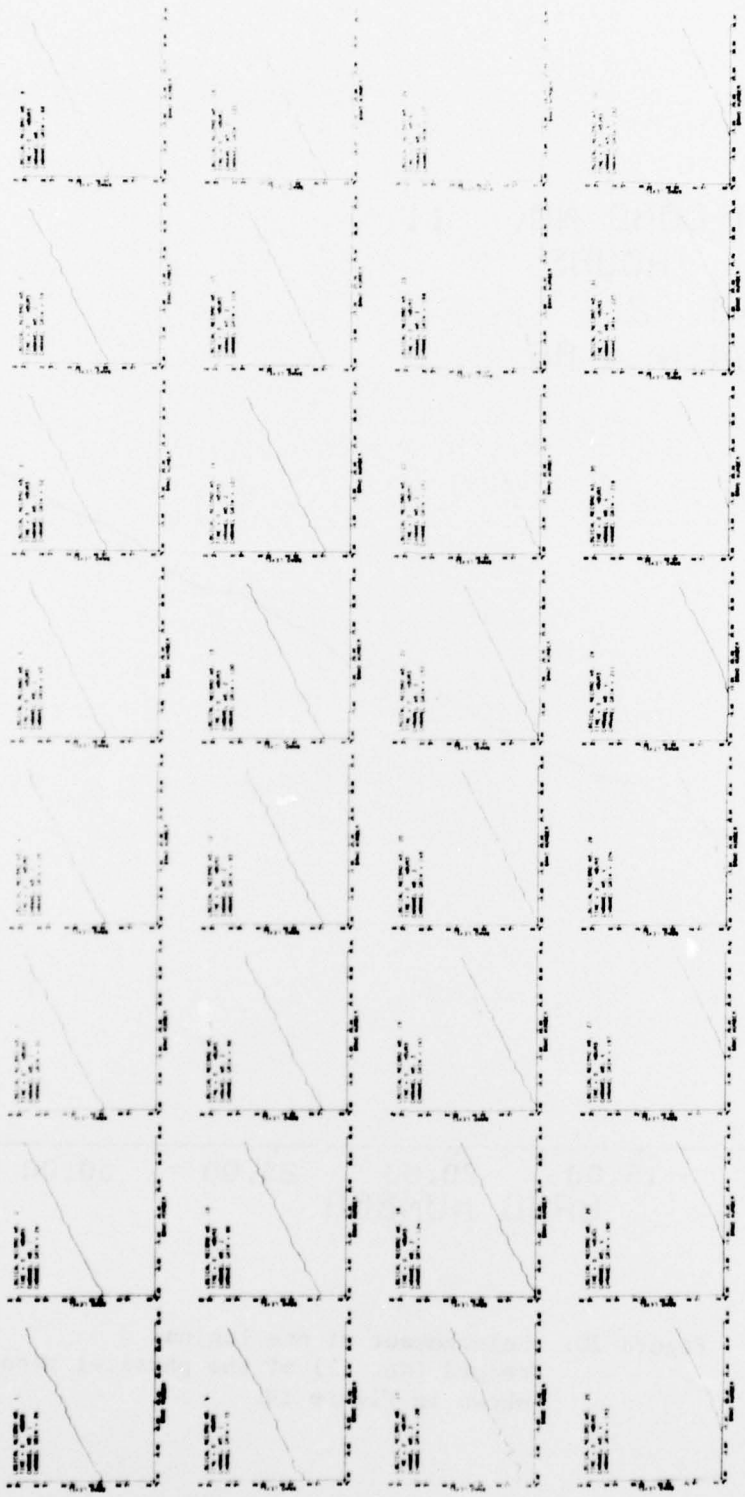


Figure 19. Example plot of one physical record. Input is the output from a white-noise generator whose level differs for each of the four channels.

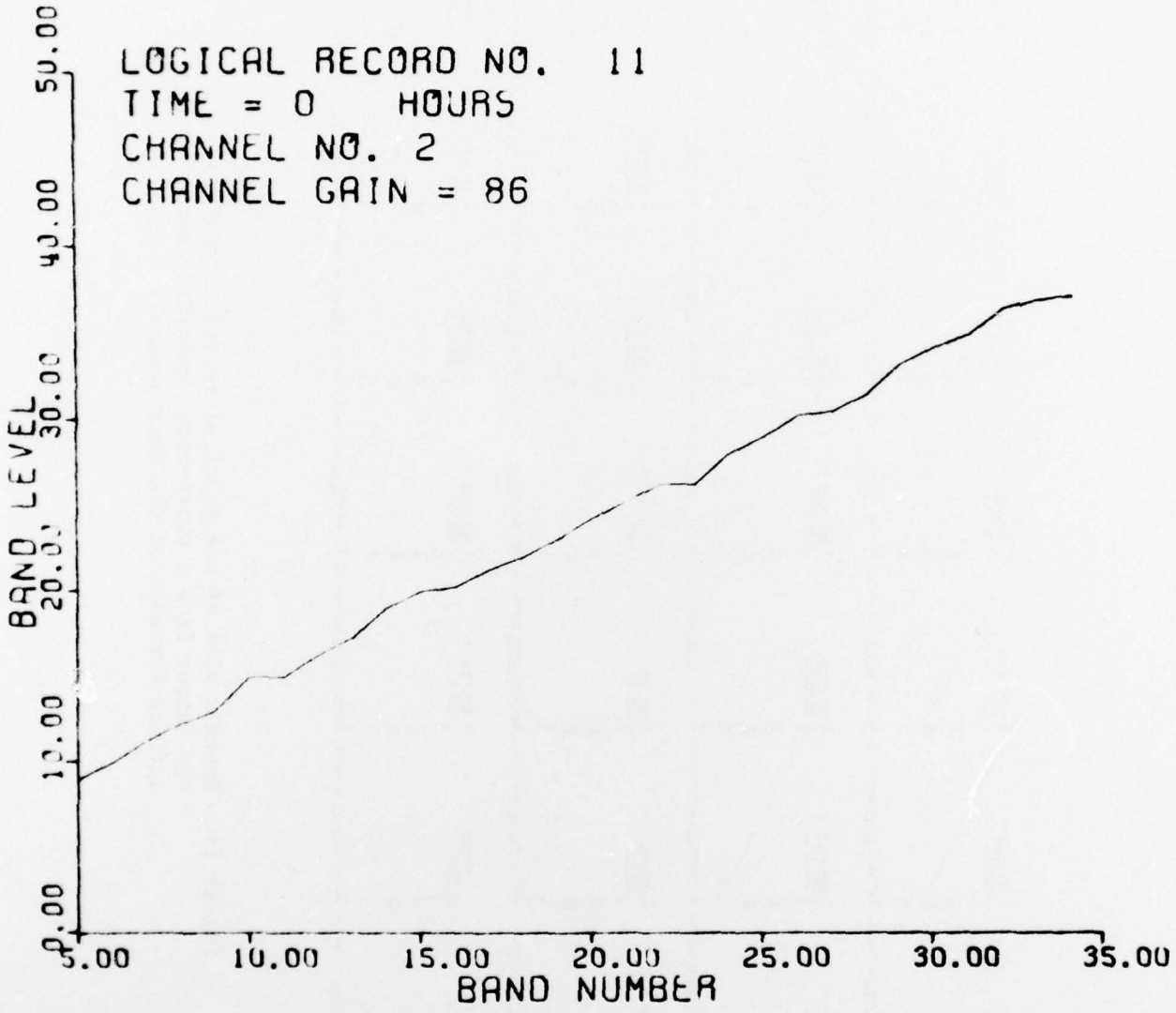


Figure 20. Enlargement of one logical record (No. 11) of the physical record shown in Figure 19.

APPENDIX A

```
C       GR ANALYZER DATA (8X4 BLOCK)
        DATA NAME /'WEIR'/
        CALL PLTNAME (NAME,4)
        DIMENSION IBUFF(1096),LOGCLR(70),BANDNO(33),BANDLL(32),GAIN(33),
       >VOLTS(33)
        CALL LIMIT(0.0,120.0,0.0,29.0)
        X=0.0
        Y=23.0
        LSKIP=0
        CALL POSREC(110,LSKIP)
        TIME=32.0*LSKIP/60.0
        INDIC=0
        J=1
        DO 12 IMP=1,4
        DO 11 INK=1,8
        L=J-1
   10   CALL READLG (IBUFF,LOGCLR,INDIC,&100)
        IF(LOGCLR(4).LE.2)CHANNO=LOGCLR(4)
        IF(LOGCLR(4).EQ.4)CHANNO=3
        IF(LOGCLR(4).EQ.8)CHANNO=4
        CHANG1=1.0*LOGCLR(7)
        CHANG2=1.0*LOGCLR(8)
        IF (J.EQ.1) GO TO 2
        GAIN(L)=CHANG1
        VOLTS(L)=-8.0+0.5*(L)
    2   CONTINUE
        M=8
        N=1
        DO 3 JAY=5,34
        BANDNO(N)=1.0*LOGCLR(M)
        M=M+2
        N=N+1
    3   CONTINUE
        M=9
        K=1
        DO 5 KAY=5,34
        BANDLL(K)=(LOGCLR(M)/100.0)
        M=M+2
        K=K+1
    5   CONTINUE
        RECLOG=1.0*(32-INDIC)
        WRITE(108,400)(RECLOG,TIME,CHANNO,CHANG1,CHANG2,BANDNO(I),
       >BANDLL(I),I=1,30)
  400   FORMAT(' ',5F10.2,I8,F10.2)
```

```
      CALL PLOT (X,Y,-3)
      BANDN8(31)=5.0
      BANDN8(32)=5.0
      BANDLL(31)=0.0
      BANDLL(32)=10.0
      CALL AXIS (0.0,0.0,'BAND NUMBER',-11,6.,0.,BANDN8(31),BANDN8(32))
      CALL AXIS (0.,0.,'BAND LEVEL',10,5.0,90.,BANDLL(31),BANDLL(32))
      CALL LINE (BANDN8,BANDLL,30,1,0,0)
      X=0.0
      Y=0.0
      W=X+0.3
      V=Y+4.75
      CALL SYMBOL (W,V+0.25,0.14,'LOGICAL RECORD NO.',0.0,18)
      CALL NUMBER (W+2.8,V+0.25,0.14,RECLOG,0.0,-1)
      CALL SYMBOL (W, V, 0.14, 'TIME =', 0.0, 6)
      CALL NUMBER (W+1.0,V,0.14,TIME,0.0,-1)
      CALL SYMBOL (W+1.6,V,0.14,'HOURS',0.0,5)
      CALL SYMBOL (W,V-0.25,0.14,'CHANNEL NO.',0.0,11)
      CALL NUMBER (W+1.7,V-0.25,0.14,CHANNO,0.0,-1)
      CALL SYMBOL (W,V-0.5,0.14,'CHANNEL GAIN =',0.0,14)
      CALL NUMBER (W+2.1,V-0.5,0.14,CHANG1,0.0,-1)
      X=X+7.0
      J=J+1
 11   CONTINUE
      X=-49.0;  Y=-7.0
 12   CONTINUE
      CALL PLOT(25.0,0.0,-3)
      GAIN(32)=0.0
      GAIN(33)=30.0
      VOLTS(32)=-8.0
      VOLTS(33)=2.0
      CALL AXIS(0.,0.,'GAIN CODE',9,8.,90.,0.,30.)
      CALL AXIS(0.,0.,'VOLTAGE LEVEL',-13,8.,0.,-8.,2.)
      CALL LINE(VOLTS,GAIN,31,1,0,0)
      IF(INDIC.EQ.0) GO TO 110
 100  CONTINUE
      IF(INDIC.EQ.-2) GO TO 110
      WRITE(108,900) INDIC
 900  FORMAT('** 100 INDIC=',I4)
 110  CALL NWPLOT
      STOP
      END
```

```
      SUBROUTINE READLG(BUFFER,LRCRD,INDIC,*)
      INTEGER*4  BUFFER(1),LRCRD(1)
      INTEGER*4 WORK(70)
      IF(INDIC.GT.0) GOTO 25
    5 CONTINUE
      CALL BUFFIN(110,1,BUFFER,1096)
   10 CONTINUE
      CALL ICHECK(110,INS,NUMBR)
      IF(INS.EQ.1) GOTO 10
      ICNT = 0
      NTOTAL = (NUMBR*4+3)/128
      IF(INS.EQ.2) GOTO 15
      INDIC = INS-5
      RETURN 1
C
   15 CONTINUE
      IF(INDIC.EQ.0) GOTO 20
      INDIC = NTOTAL
      RETURN
C
   20 CONTINUE
      INDIC = NTOTAL
   25 CONTINUE
      IF(ICNT.GE.NTOTAL) GOTO 5
C
      ILL  = ICNT*128/4
      ILLR = (ICNT*128-ILL*4)*2
      ENCODE(280,126,WORK) (BUFFER(ILL+I),I=1,35)
      DECODE(280,127,WORK) ILLR,(LRCRD(I),I=1,67)
  126 FORMAT(70Z8)
  127 FORMAT(NX,272,74,4Z2,30(I2,I6))
C
      ICNT  = ICNT+1
      INDIC = INDIC-1
C
      RETURN
      END
```